Effect of Diameter Variation on Electrical Characteristics of Schottky Barrier Indium Arsenide Nanowire Field-Effect Transistors

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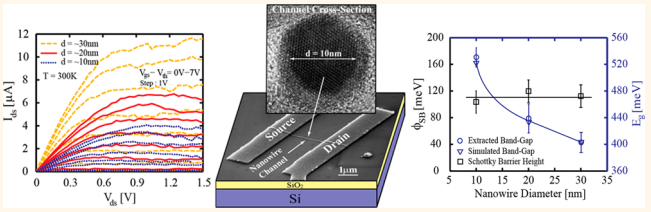
ABSTRACT The effect of diameter variation on electrical characteristics of long-channel InAs nanowire metal—oxide—semiconductor field-effect transistors is experimentally investigated. For a range of nanowire diameters, in which significant band gap changes are observed due to size quantization, the Schottky barrier heights between source/drain metal contacts and the semiconducting nanowire channel are extracted considering both thermionic emission and thermally assisted tunneling. Nanowires as small as 10 nm in diameter were used in device geometry in this context. Interestingly, while experimental and simulation data are consistent with a band gap increase for decreasing nanowire diameter, the experimentally determined Schottky barrier height is found to be around 110 meV irrespective of the nanowire diameter. These observations indicate that for nanowire devices the density of states at the direct conduction band minimum impacts the so-called branching point. Our findings are thus distinctly different from bulk-type results when metal contacts are formed on three-dimensional InAs crystals.



KEYWORDS: InAs · MOSFET · nanowire · Schottky barrier · narrow band gap · Tersoff's theory

Complementary metal—oxide—semiconductor (CMOS) scaling is turning into one of the most challenging problems that the electronics industry has come across in decades. Scaling procedures should be able to achieve the same electric-field pattern in a smaller transistor while reducing the supply voltage.[1] Among all the device candidates for conventional CMOS replacement, excellent electrostatic conditions and band gap engineering capabilities make nanowire field-effect transistors (NWFETs) a promising choice for future electronics.[2] NWFETs with large Bohr radius channel materials such as InAs[3] are particularly interesting because transition from conventional to quantum transport occurs at relatively large diameters (10—30 nm). This aspect can enable novel circuit design techniques in which designers can benefit from both conventional and low-dimensional transport properties of NWFETs on the same chip. In addition, these types of nanowires allow studying physics phenomena that are well-established in two and three dimensions for the first time in a one-dimensional system. While InAs nanowires have been identified as potential candidates for electronic applications[4—13] due to their excellent transport properties, the reality of making a device always involves contact formation. The higher the channel mobility is, the more stringent the demands on the contacts and the harder it is to truly benefit from the channel performance. To address this issue, many researchers have explored chemical wet etching/passivation or gas treatment of the contact area[14—17] and formation of InAs/metal alloys.[18] Instead, here we present a careful study on the formation of Schottky barriers (SBs) at the metal-to-InAs interface to understand the underlying physics and to provide insights into the expected performance of NWFETs with scaled diameters. With a diameter of only 10 nm, the InAs NWFETs used in this study are the smallest

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reported so far. To date, relatively little attention has been paid to the formation of SBs between metal contacts and InAs NWs mostly due to the presumption of Fermi level pinning in the conduction band of InAs. This study demonstrates that the assumption of Ohmic contact formation between source/drain (S/D) metal contacts and InAs channels due to Fermi level pinning in the conduction band does not hold for InAs NWs, which exhibit a confinement of the electron wave function in two dimensions. Even though device characteristics show a linear dependence between I_{ds} and V_{ds}, as shown in Figure 1, which is often wrongfully interpreted as evidence of an Ohmic contact,[19,20] SBs of finite height form at the metal-to-channel interface. Interestingly, we find that Schottky barrier heights (Φ_{SB}) are independent of the nanowire diameter (*i.e.*, band gap), a finding that will be discussed in greater detail below.

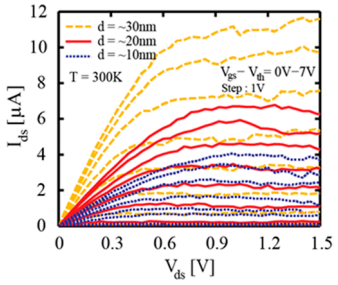

Figure 1. Output characteristics of back-gated single InAs NWFETs for three different NW diameters. The drain current increases monotonically with diameter for the same overdrive voltage.

RESULTS

Schottky Barrier Extraction. In metal−oxide−semiconductor field-effect transistors (MOSFETs), charge transport between source and drain is directly related to the details of the potential profile along the channel. Presence of a SB between the S/D metal contacts and the semiconducting channel alters this profile and limits the current, both in the on-state and the near-threshold region. As illustrated in Figure 2a, variable temperature-dependent transfer characteristics have been used to extract the Φ_{SB}.[21] Devices exhibit three regions of operation depending on the gate voltage (V_{gs}). In the on-state ($V_{gs} > V_{th}$) for modest drain voltages, the primary conduction mechanism is thermally assisted tunneling through the source/channel SB. Note that the barrier thickness and thus the tunneling probability through the barrier is a function of V_{gs}. Two regions of operation are observed for the off-state ($V_{gs} < V_{th}$). For gate biases near threshold ($V_{FB} < V_{gs} < V_{th}$), it is still the gate voltage dependence of the tunneling component that results in a change of current flow through the device and determines the subthreshold slope.[22,23] For sufficiently negative gate voltages ($V_{gs} < V_{FB}$), thermionic emission over the barrier is the only allowed transport mechanism and

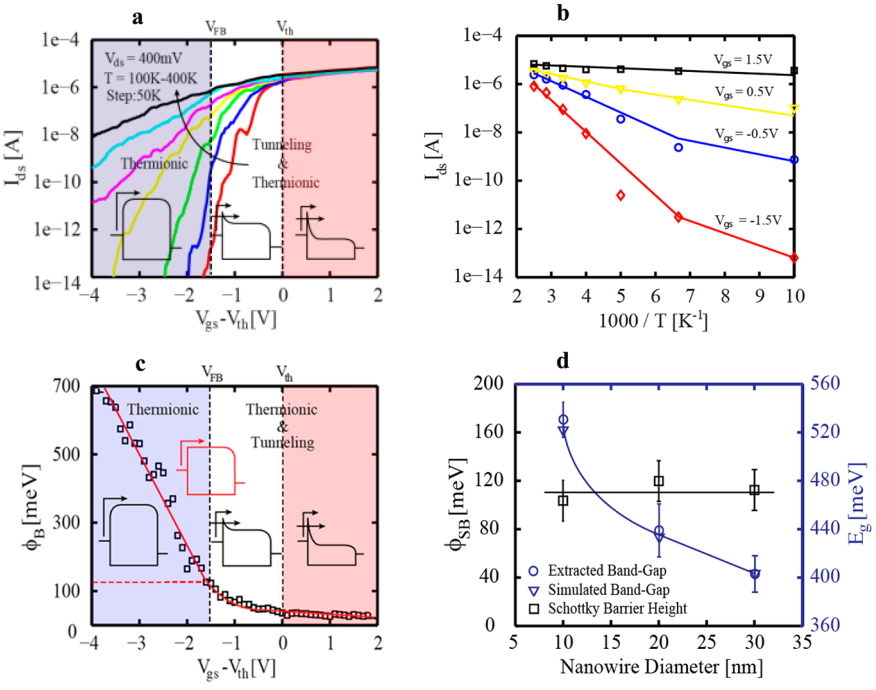

Figure 2. (a) Temperature-dependent transfer characteristics of a back-gated InAs NWFET. The band diagrams illustrate the contributions of $I_{thermionic}$ and $I_{tunneling}$ for different bias conditions. Measurements were performed at V_{ds} = 400 mV. (b) Corresponding Arrhenius plots for various gate voltages. (c) Barrier height extracted from (b) showing the transition from thermionic to thermionic/tunneling behavior, as illustrated in the graph. (d) Extracted SB heights and band gap values inferred from V_{th} shifts ("extracted") and band structure simulation ("simulated") for various nanowire diameters. The extracted band gap results are in good agreement with simulations.

the device enters its conventional bulk controlled off-state. The transition between the thermally assisted tunneling and the thermionic emission regime can be used to determine Φ_{SB}. Figure 2a shows the measured subthreshold characteristics of an InAs device at various temperatures. As discussed above, the current from source to drain consists, in general, of two components, a thermionic emission ($I_{thermionic}$) and a thermally assisted tunneling ($I_{tunneling}$) current, which are illustrated as insets in Figure 2a. The corresponding Arrhenius plots are shown for various V_{gs} values in Figure 2b. If the flat-band voltage (V_{FB}) is identified correctly, then conventional thermionic emission theory (see eq 1[24]) can be used in the high-temperature region to extract the activation energy, that is, the actual barrier height (Φ_B) (see Figure 2c).

$$I_{DS} = A^* T^2 \exp(-(q\Phi_B)/(k_B T))[1 - \exp(-(qV_{DS})/(k_B T))] \quad (1)$$

where A^* is the Richardson's constant, k_B is the Boltzmann constant, q is the charge of an electron, and T is the temperature. For V_{gs} values corresponding to channel potentials below flat-band ($V_{gs} < V_{FB}$), $\Phi_B = \Phi_{SB} + \beta(V_{gs} - V_{FB})$, where β is a voltage scaling factor that can be extracted from the comparison of the experimental subthreshold slope of each device with the ideal subthreshold slope of 60 mV/decade. For V_{gs} values within the region where tunneling plays a significant role, applying eq 1 results in effective barrier heights smaller than Φ_{SB}. Equation 1 also indicates that barrier heights must been extracted at high enough V_{ds} to ensure that the SB at the drain side is cleared and does not affect the analysis. Unlike the channel energy, bands at the drain move one to one with V_{ds} due to the physical nature of the metal/semiconductor contact. Since the average Schottky barrier height at the contacts is ~110 meV, applying 110 mV of drain voltage is enough to remove the unwanted barrier. All measurements are done at V_{ds} = 400 meV, which guarantees that the drain Schottky barrier does not exist. Figure 2c plots Φ_B inferred from the slopes in Figure 2b *versus* V_{gs} for the same device. Three regions of operation are clearly observed in Figure 2c, corresponding to the diagrams in the insets. For sufficiently negative gate voltages, where $I_{thermionic}$ is the only current component, Φ_B is a linear function of V_{gs}. At a $V_{gs} - V_{th}$ of ~−1.5 V, a clear change in slope is observable. This transition is attributed to the contributions of $I_{tunneling}$. The V_{gs} value at which this deviation occurs is V_{FB} of the device, and Φ_B at this voltage is the actual Schottky barrier height Φ_{SB}. Figure 2d presents the extracted Φ_{SB} values for three nanowire diameters, along with band gaps obtained from band structure calculations and inferred from various measurements (discussed later). A Φ_{SB} of around ~110 meV is observed for all nanowire diameters in this study—a surprising result considering the substantial change in band gap with nanowire diameter (see below).

DISCUSSION

Traditionally, Fermi level pinning in planar systems has been associated with surface states, intrinsic interface states, or defects in the semiconductor.[25−32] Surface states that pin the Fermi level (E_F) define the branching point (E_B),[33] which tends to lie near the center of the band gap.[34] Although in the majority of III−V materials, including InAs, the direct band gap is determined by the conduction band minimum (E_C) at the Γ-valley, Tersoff's theory explains how Fermi level pinning occurs in the middle of the indirect band gap (E_i) at the L-valley instead.[35,36] In the case of bulk InAs, E_B is located energetically above the minimum of the conduction band at the Γ-valley, which implies that the Fermi level is pinned in the conduction band rather independent of the metal work function.[33,37] Accordingly, one would expect negligible SBs at the metal-to-InAs interface if devices behave bulk-like. On the other hand, if strong quantization impacts the direct band gap in an InAs nanowire, one might expect that the effective SB for electron injection into the InAs channel increases with decreasing diameter since states of the indirect conduction band, which remains almost unaffected by size quantization effects, keep the energetic distance between the valence band maximum and E_B almost the same as in the planar case. Both of the above statements are not supported by experiments. The first statement is inconsistent with experimental results on InAs nanowires that show frequently high contact resistance values in the 50 to 100 kΩ range (see Figure 1 and refs 14, 15, and 18). The second is inconsistent with our data presented in Figure 2d that clearly reveal the trend of increasing band gap with decreasing wire diameter but do not show any substantial change of Schottky barrier height. We propose that strong quantization in ultrasmall InAs nanowires as studied here, as well as the particular electrostatics of a wire geometry, impact the location of E_B relative to the conduction band edge at the Γ-valley substantially, a fact that has not been noted before nor carefully studied experimentally. Note in this context that Leonard and Tersoff discussed how in the case of a metal/nanotube contact the situation is radically different from the planar case; that is, screening in an ideal one-dimensional system results in an unpinned junction.[38] As an extension of this argument, we submit that for a low-dimensional nanowire system the position of E_B is determined by both conduction band states at the Γ-point and the actual S/D metal work function. Our experimental results on the Schottky barrier heights for different nanowire diameters (discussed above) in conjunction with our analysis of the impact of NW diameter on the band gap (presented below) provide first time evidence for this

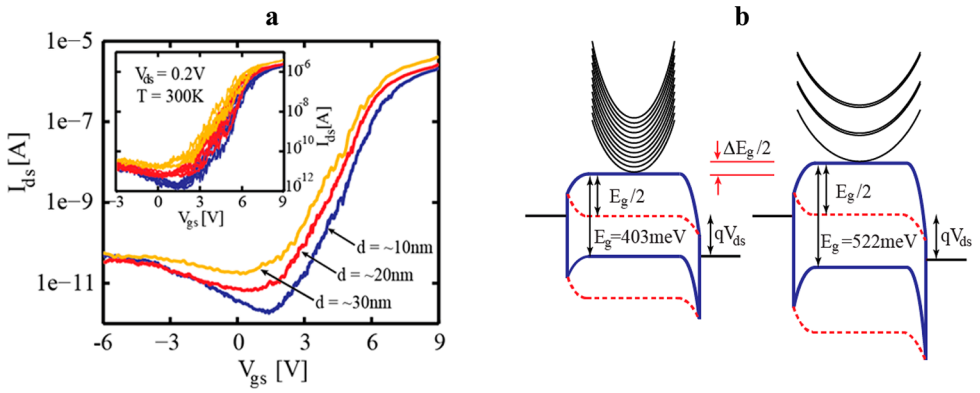

Figure 3. (a) Measured transfer characteristics for back-gated InAs NWFETs, with each curve representing the average over multiple measurement sweeps. The inset shows the original measurements. (b) Band diagrams with solid lines are illustrating the condition in which the source Fermi level is lined up with midgap for the largest (left) and the smallest (right) NWs. Calculated $E-k$ relationships for the respective one-dimensional sub-bands are also shown. The shift in threshold voltage between these devices (ΔV_{th}) corresponds to the difference in gate voltage required to move the bands to a point where $E_C \sim E_F$, *i.e.*, threshold. Band diagrams with dashed lines show the devices biased at threshold.

claim but certainly need more rigorous theoretical analysis to identify the underlying physics in highly quantized nanowire systems.

Band Gap Extraction. To provide evidence for our above stated claim of band gap change with nanowire diameter, two different approaches are presented in the following subsections. These methods are combining our experimental results with simulations in order to verify that the band gap is substantially changing for NWs in the diameter range of 10 to 30 nm.

Band Gap and Threshold Voltage Shift. In this subsection, the simulated band gap for InAs NWs with the largest diameter (see Figure 4a, left panel) is used as the starting point to extract the band gaps for smaller diameter devices. Simulations were performed using a tight-binding approach in the NEMO 5.0 software package.[39] In particular, the threshold voltage shift (ΔV_{th}) of NWFETs with different channel diameters is translated into a band gap change of the respective device. Figure 3a shows slightly ambipolar subthreshold characteristics for devices with various channel diameters. Measurements are averaged over many sweeps to suppress fluctuations in V_{th} caused by substrate charging, humidity, *etc.*[40] The inset of Figure 3a shows the original set of measurements. It is apparent that V_{th} increases when the NW diameter is reduced; that is, the band gap is increased. The observed change in threshold (ΔV_{th}) can be used to quantitatively infer the band gap difference between channels with different diameters. If we assume that the doping density in the different wires is similar,[41] any increase in band gap will result in a positive threshold voltage shift for the *n* branch of the subthreshold characteristics that corresponds to half of the band gap change ($\Delta E_g/2q$), as illustrated in Figure 3b. In this context, the blue band diagrams for the large and small NW diameter illustrate the situation at the same gate voltage deep in the device off-state below threshold, and the red dashed lines show the situation at threshold. Knowing the voltage scaling factor β from the subthreshold slope to convert the change in V_{th} for two different NW diameters into a corresponding change in channel potential at threshold can then be used to deduce the band gap for NWs with 20 and 10 nm diameter based on the calculated band gap for 30 nm NWs, which is 403 meV according to Figure 4a (left panel). Since the largest diameter NW has the smallest band gap (*i.e.*, resembles bulk InAs the most), using this band gap as reference ensures the smallest error in our extraction. Using this approach, the ΔV_{th} between 30 and 20 nm devices (~270 mV) converts to $\Delta E_g/2$ of ~18 meV, yielding a band gap for the 20 nm device of ~439 meV. Similarly, the extracted band gap for the 10 nm NWFET is found to be ~531 meV. Figure 2d shows that the extracted band gap values using the above ΔV_{th} method are in good agreement with the simulation results shown in Figure 4a. Error bars in Figure 2d were obtained by considering one standard deviation using the repeated measurements in Figure 3a.

Band Gap and Size Quantization. This subsection links the band structure simulation results for NWFETs with various channel diameters with low-temperature experimental transfer characteristics in order to provide further evidence for the diameter-dependent band gap in InAs. Figure 4a shows calculated band structure results for NWs with various diameters. A systematic increase in band gap for NWs with diameters of ~30, ~20, and ~10 nm from 403 to 433 meV to 522 meV is observed.[42] Figure 4b shows the energies of the first 10 conduction sub-band minima for the same NW diameters. The energy differences between the first two sub-bands (ΔE) for 10, 20, and 30 nm NWs are ~150, ~70, and ~39 meV, respectively. Typically, if ΔE is larger than about $4k_BT$, individual one-dimensional

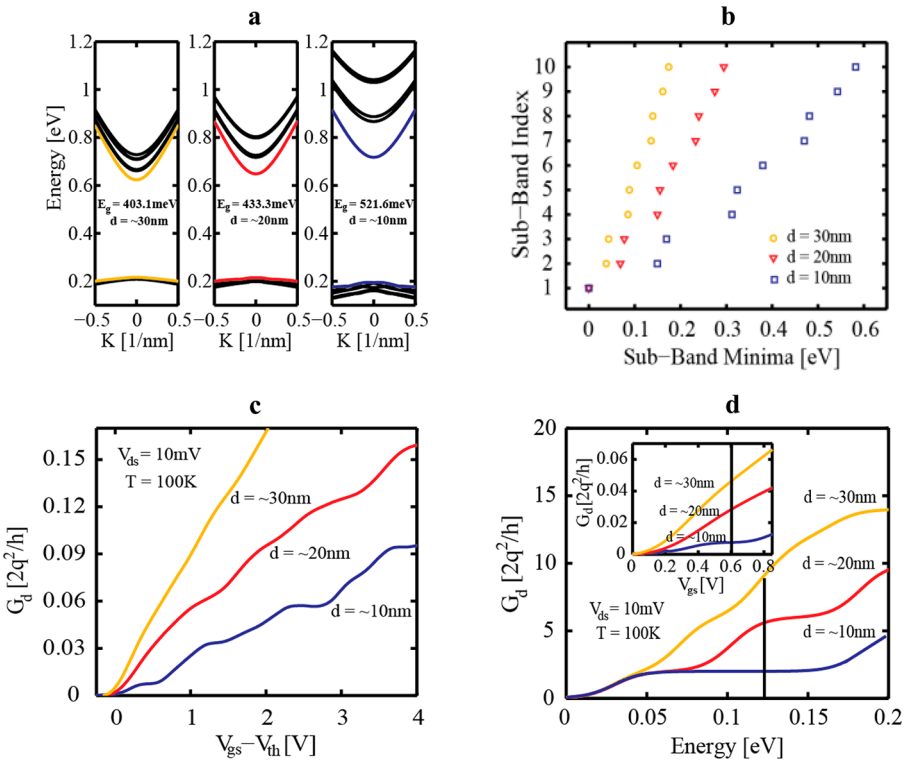

Figure 4. (a) Band structure simulation for InAs NWs with diameters of 30, 20, and 10 nm. (b) Sub-band energies with respect to the first conduction band minimum for NWs of part a. (c) Measured low-temperature conductance for InAs NWFETs with different diameters. Quantum effects are visible for smaller devices.[44] (d) Simulated conductance for InAs NWFETs with diameters of 30, 20, and 10 nm. The inset is a zoom of part c.

(1D) modes can be resolved.[43] Figure 4c shows measurements of transfer characteristics at 100 K ($4k_BT \propto 35$ meV) for NWFETs with similar diameters as considered in Figure 4a. Contributions from individual 1D modes can be clearly distinguished for the smallest NWFET and become less pronounced for increasing wire diameter, consistent with the expectations from the simulations. To provide further quantitative proof of the agreement between simulations and experiments, the measured transfer characteristics of Figure 4c are compared with their simulated counterparts.

Figure 4d shows the simulated conductance values using the Landauer formalism (see eq 2 and ref 45) for transistors with similar channels as Figure 4a.

$$I_d = \frac{2q^2}{h}\int_0^\infty T(E)\cdot M(E)\cdot[f_S(E) - f_D(E)]\cdot dE \qquad (2)$$

where $T(E)$ is the transmission coefficient, $M(E)$ is the number of modes, and $f_{S,D}(E)$ represents the source and drain Fermi distributions. In Figure 4d, ballistic transport (*i.e.*, $T(E) = 1$) has been assumed. When simulated results are compared with our experimental findings (inset of Figure 4d), various strong similarities are observed. In particular, the 10 nm diameter wire results (experimental and simulations) both indicate a saturation of conductance due to only one one-dimensional mode contributing over a sizable gate voltage (energy) range. Note that the absolute conductance values are dissimilar since scattering is not included in the simulations. Furthermore, conductance ratios at a given voltage (energy) range are very similar, indicating that, in fact, an almost constant scattering rate is the main

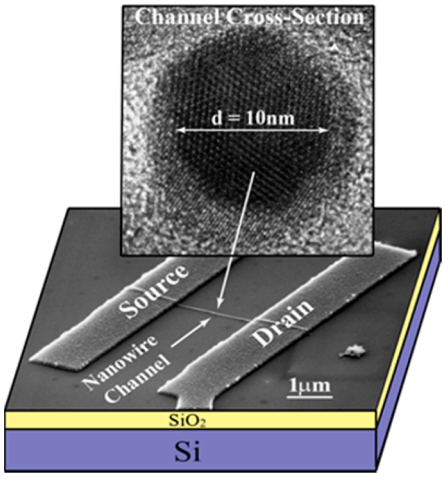

Figure 5. Tilted SEM image of an InAs NWFET. S/D contacts and channel lengths are 1 and 1.6 μm, respectively, to avoid any contact length related or short-channel effects in the electrical characteristics. The cross-sectional high-resolution TEM of the channel is shown for the thinnest NW channel with a hexagonal cross section. A 2−3 nm native oxide wraps around the entire NW channel.

difference between the simulation and experimental results:

$$\frac{G_{d-20\text{nm}-\text{experiment}}}{G_{d\ -\ 10\text{nm}-\text{experiment}}} \cong \frac{G_{d-20\text{nm}-\text{simulation}}}{G_{d-10\text{nm}-\text{simulation}}}$$

$$\frac{G_{d-30\text{nm}-\text{experiment}}}{G_{d-20\text{nm}-\text{experiment}}} \cong \frac{G_{d-30\text{nm}-\text{simulation}}}{G_{d-20\text{nm}-\text{simulation}}}$$

The above ratios are illustrated by the vertical lines in Figure 4d for a specific channel potential and in the inset for a V_{gs} value that corresponds to the channel potential. The connection between the gate voltage and energy scale in the device on-state is not through β as described in the context of the off-state discussion previously (see Band Gap and Threshold Voltage Shift section). Instead, an approximate quantum capacitance value has been used to identify the energy value in Figure 4d that corresponds approximately to a gate voltage of 0.6 V (see inset).

CONCLUSION

In summary, we have provided first time experimental evidence for an unusual behavior of Schottky barrier formation in ultrasmall InAs nanowires. Our experimental results indicate that while a clear change of the band gap with diameter as expected from simulations occurs and size quantization results in one-dimensional modes consistent with the dimensions of the wires, Schottky barriers of around 110 meV for Ni contacts are found independent of wire diameter. This observation is not readily understandable within the framework of surface states in planar InAs devices but rather occurs to be a result of the low dimensionality and particular electrostatics of our nanowire transistors.

EXPERIMENTAL SECTION

The InAs NWs used in this study were synthesized by metal-organic chemical vapor deposition (MOCVD), on a silicon (111) substrate, through the Au-assisted vapor−liquid−solid (VLS) mechanism.[46−48] NWs have diameters of ∼10−30 nm and are surrounded by a native oxide shell of 2−3 nm, as shown in the high-resolution TEM image of Figure 5.

For device fabrication, the NWs are detached from the growth substrate by sonication in isopropyl alcohol. The NW suspension is then drop-cast onto a p^+ silicon substrate with a 20 nm thermally grown oxide (SiO_2) which serves as the global back-gate and gate dielectric, respectively. S/D contacts are defined using electron-beam lithography, followed by a ∼6 s etch in 10:1 diluted BOE solution to remove the InO_x/AsO_x native oxides in the contact regions and electron-beam evaporation of Ni. Figure 5 shows a tilted SEM image of the fabricated device and a high-resolution cross-sectional TEM image of the channel region with a ∼10 nm diameter NW.

Conflict of Interest: The authors declare no competing financial interest.

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